Radiation tolerant pixel FE in the TSMC 0.25µ process

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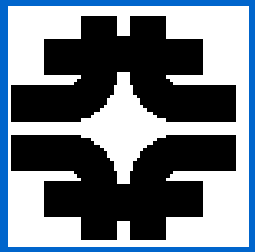
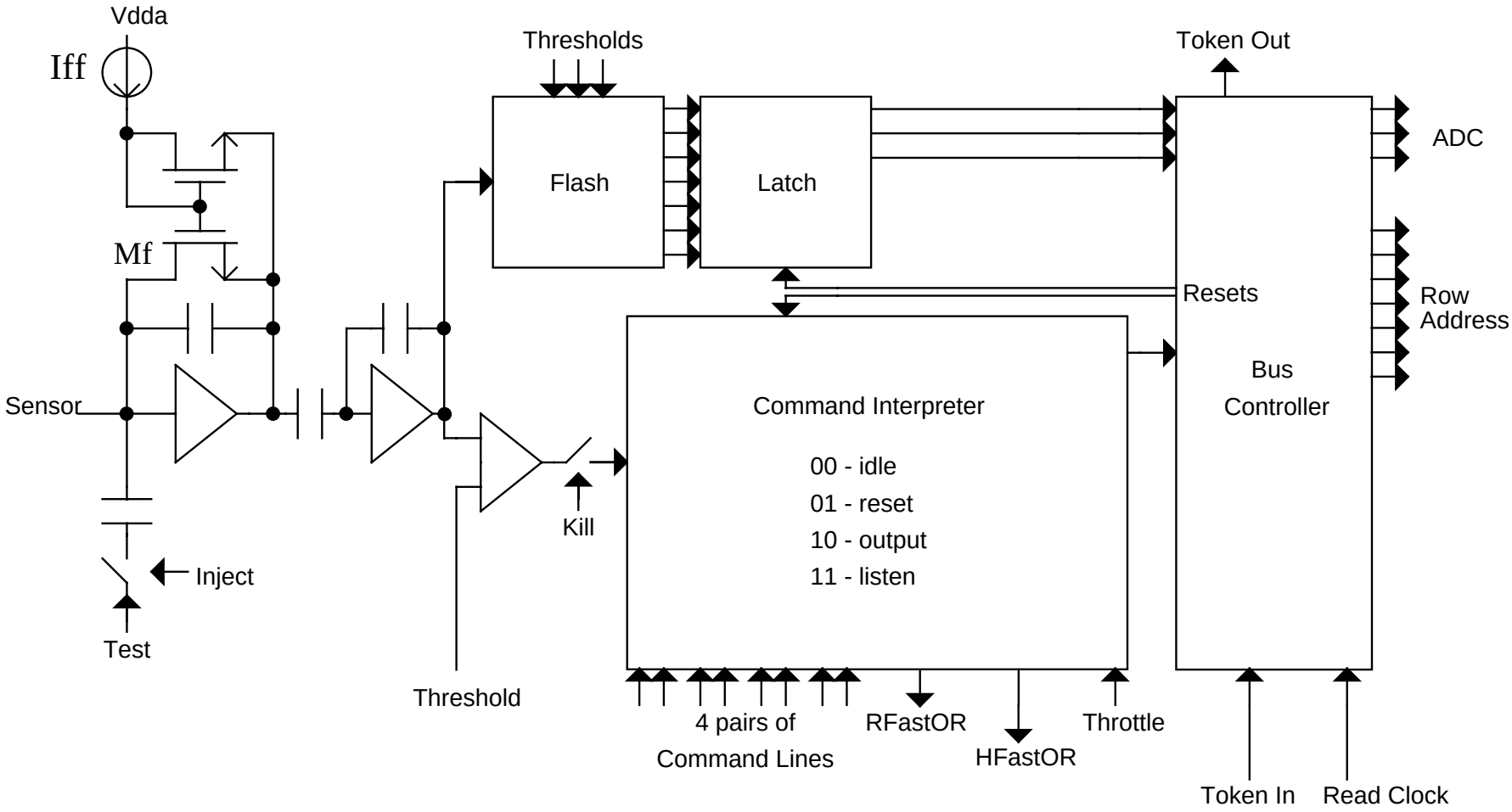


Fermilab

FPIX History

- 1997: FPIX0, a 12X64 HP 0.8u process
  - Two stage front-end, analog output digitized off chip
  - A data driven non-triggered RO
  - Successfully used in beam tests
- 1998: FPIX1, a 18X160 Hp 0.5u process
  - Two stage front-end, with one 2b FADC/cell.
  - Fast triggered/non triggered RO
  - successfully used in beam tests
- 1999: preFPIX2_T, 2X160 TSMC 0.25u (to be presented today)
  - Radiation tolerant techniques forced us to design a new front-end with a new leakage compensation strategy.
- 2000: preFPIX2_I, 18X32 0.25u CERN process (In fab)
  - Same as FE cell as in preFPIX2_T but with compelete fast non-triggered RO.

FPIX1 front-end



See the proceedings of the 1999 workshop on the electronics for the LHC (Snowmass) and references therein.

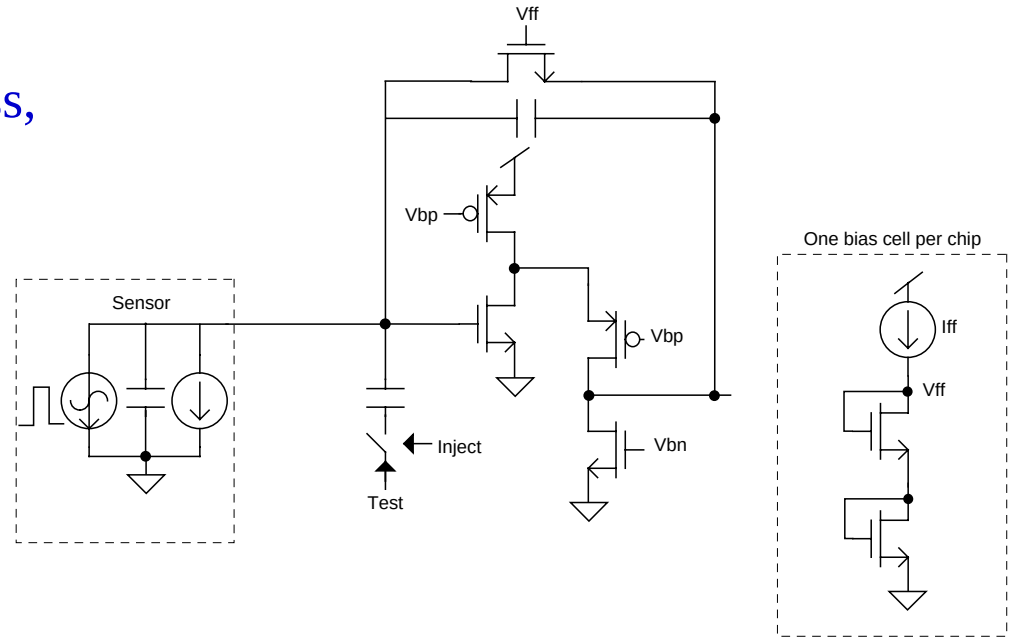
Main radtol design constraints

- The feedback structure used two NMOS devices and a biasing PMOS device (as a current source Iff).
- In the previous design: stability, noise and proper shaping relied on having a long (W/L << 1) N-channel device in the feedback (Mf).
- Leakage current tolerance insured by the feedback structure.
- Problems to implement present DSM radtol design:
  - NMOS in 0.25µ has higher transconductance than in 0.5µ process.
  - Minimum enclosed NMOS has W/L around 5. (See the RD49 reports.)
  - Enclosed NMOS with its required guard ring occupy large area.

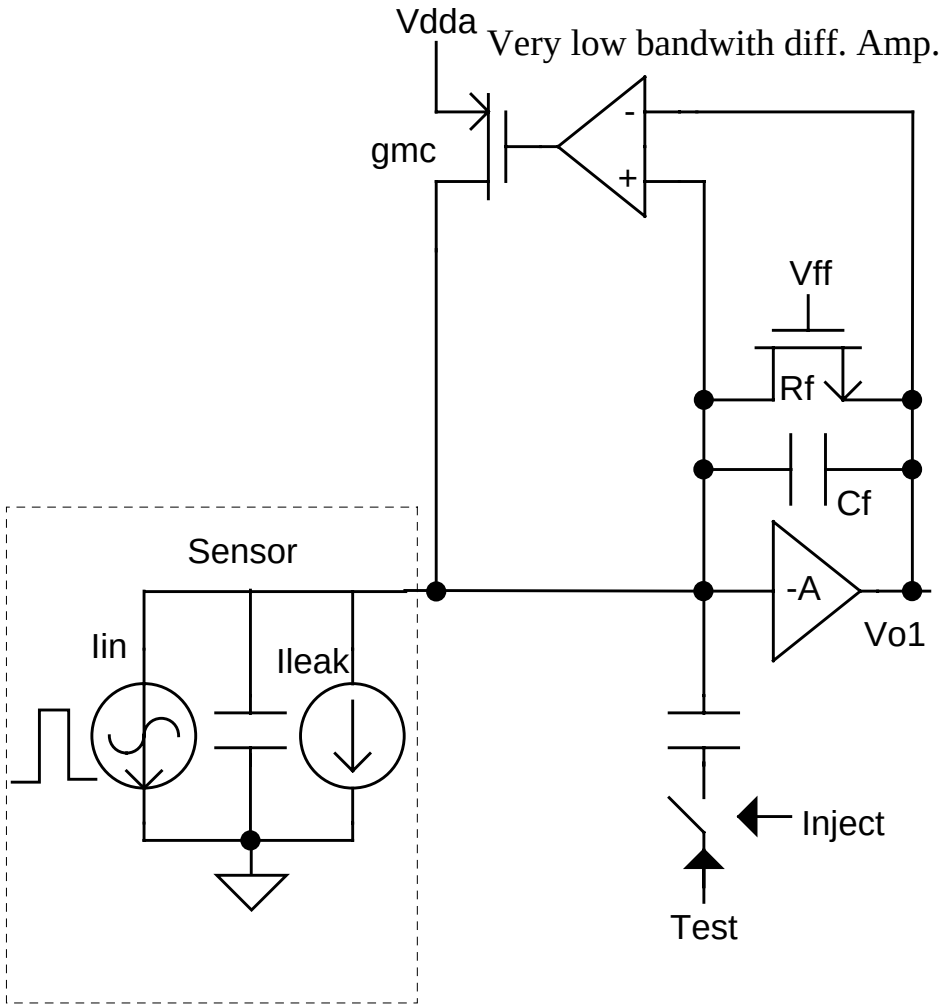
It's quasi impossible to implement the present design in the available area.

Feedback solution

- One NMOS feedback transistor biased by a global voltage VFF.
- VFF generated such as to track (to the 1st order) the preamp DC level shifts due to global changes (process, temperature…)
- Feedback is current controlled as before. This current can be much higher than in the previous scheme.
- It is more reliable to work with higher currents.
- Leakage current compensation assured by a separate scheme (next slide).



Leakage current compensation scheme



Very low bandwith diff. Amp. Ideally: $H(s) = \frac{A_{0c}}{s}$

Simplistic analysis yields:

$$\frac{Vo1(s)}{Ii(s)} = \frac{1}{Cfs + gf + \frac{A_{0c} g_{mc}}{s}}$$

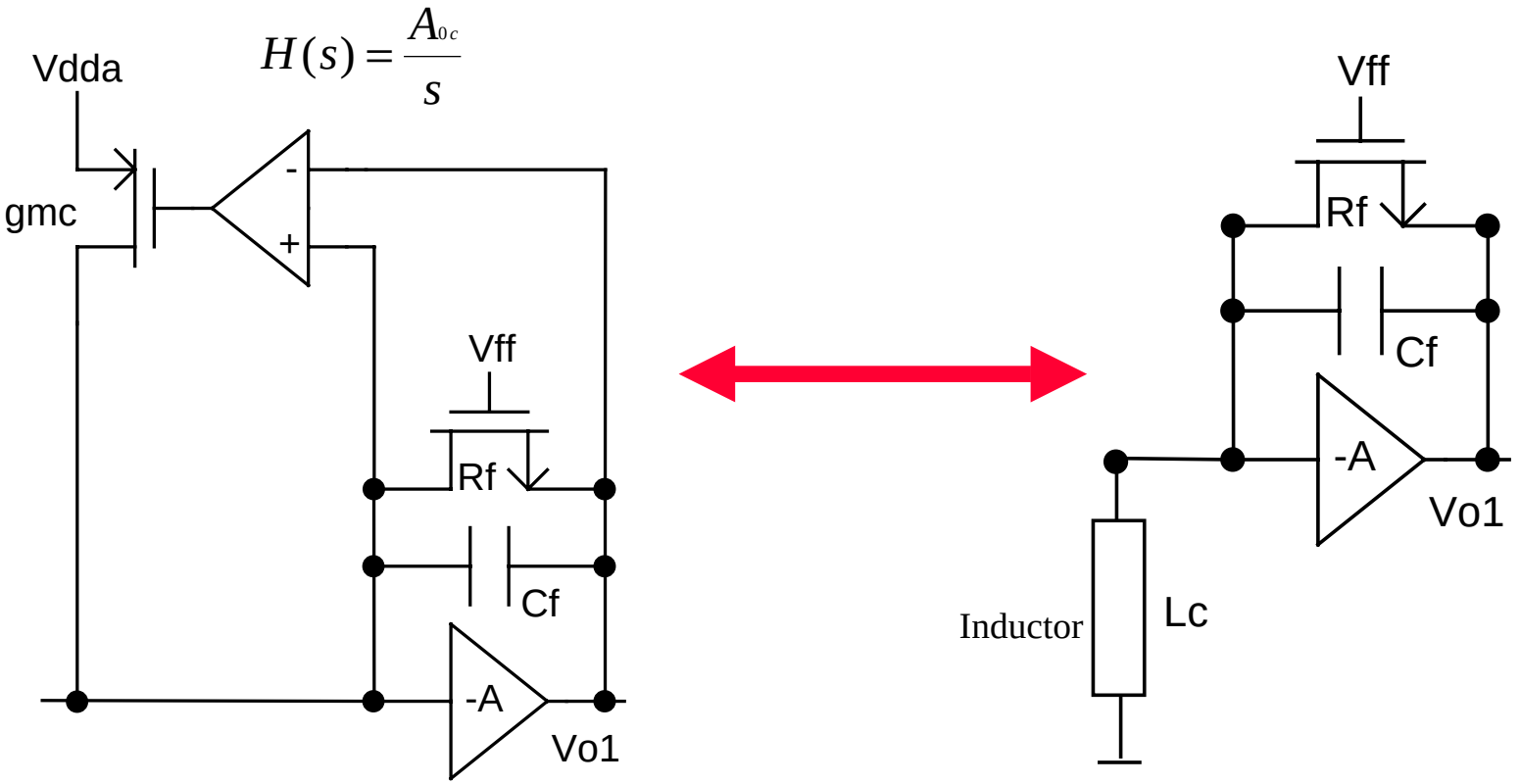
$$\frac{Vo1(s)}{Ii(s)} = \frac{s}{C_f\left(s^2 + g_f s + \frac{1}{LC_f}\right)}$$

S = Laplace variable

=> Compensates only one polarity.

=> The new scheme, though more complexe, occupy a modest area

Leakage current compensation scheme



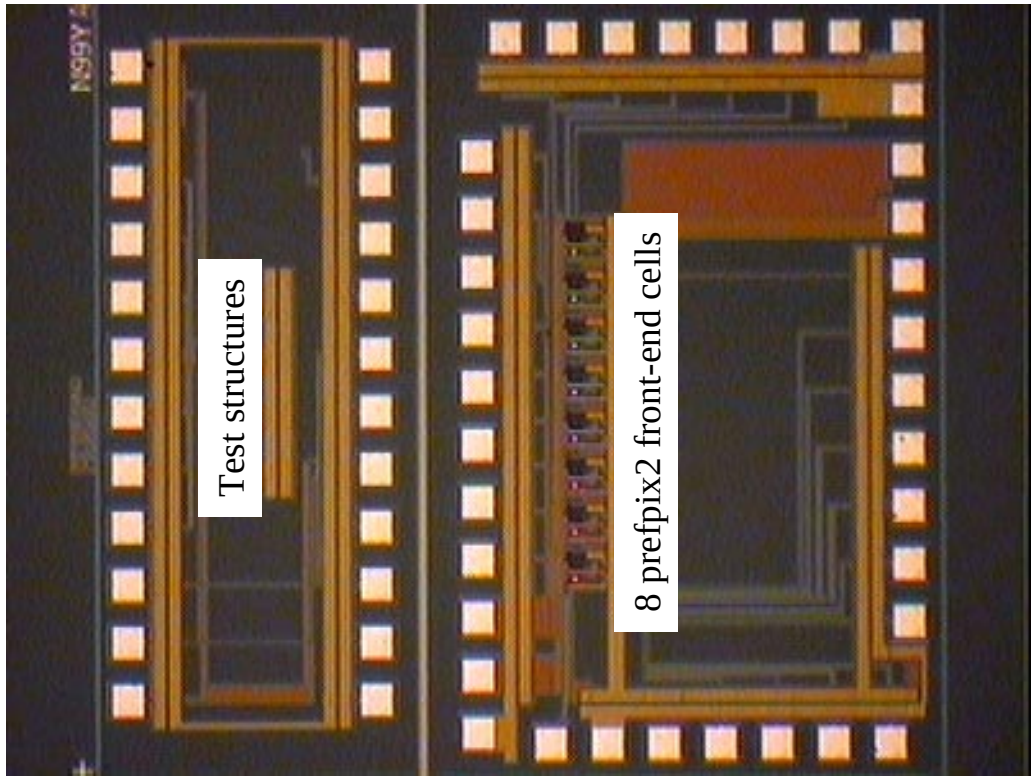
TSMC && the “CERN process”

- After some comparative work we decided to constrain our design to work well whether implemented in the “CERN” or TSMC process.
- Minor additional layout is required to submit to both processes (mostly through automatic generation)
- TSMC is offered by MOSIS (4 runs/year). 6 runs/yr is planned.
- It is wise to have a 2nd source for production.

=> CERN process is the process selected by CERN to implement their deep sub-micron radtol designs.

preFPIX2

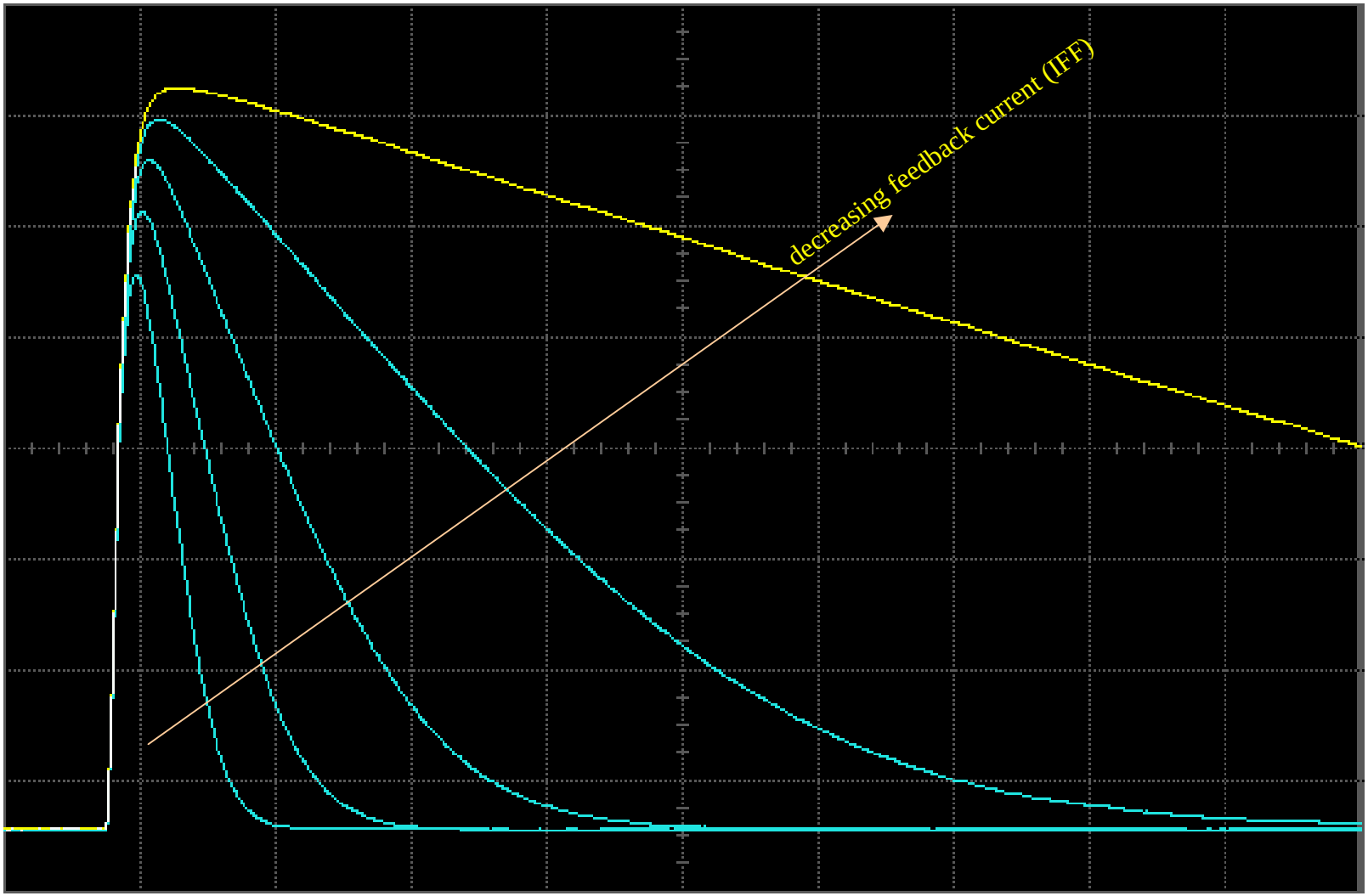
- preFPIX2 is the first prototype we designed to investigate our ideas and to test the radiation hardness of the TSMC 0.25µ process. It contains 8 pixel front-end cell and several isolated transistor.



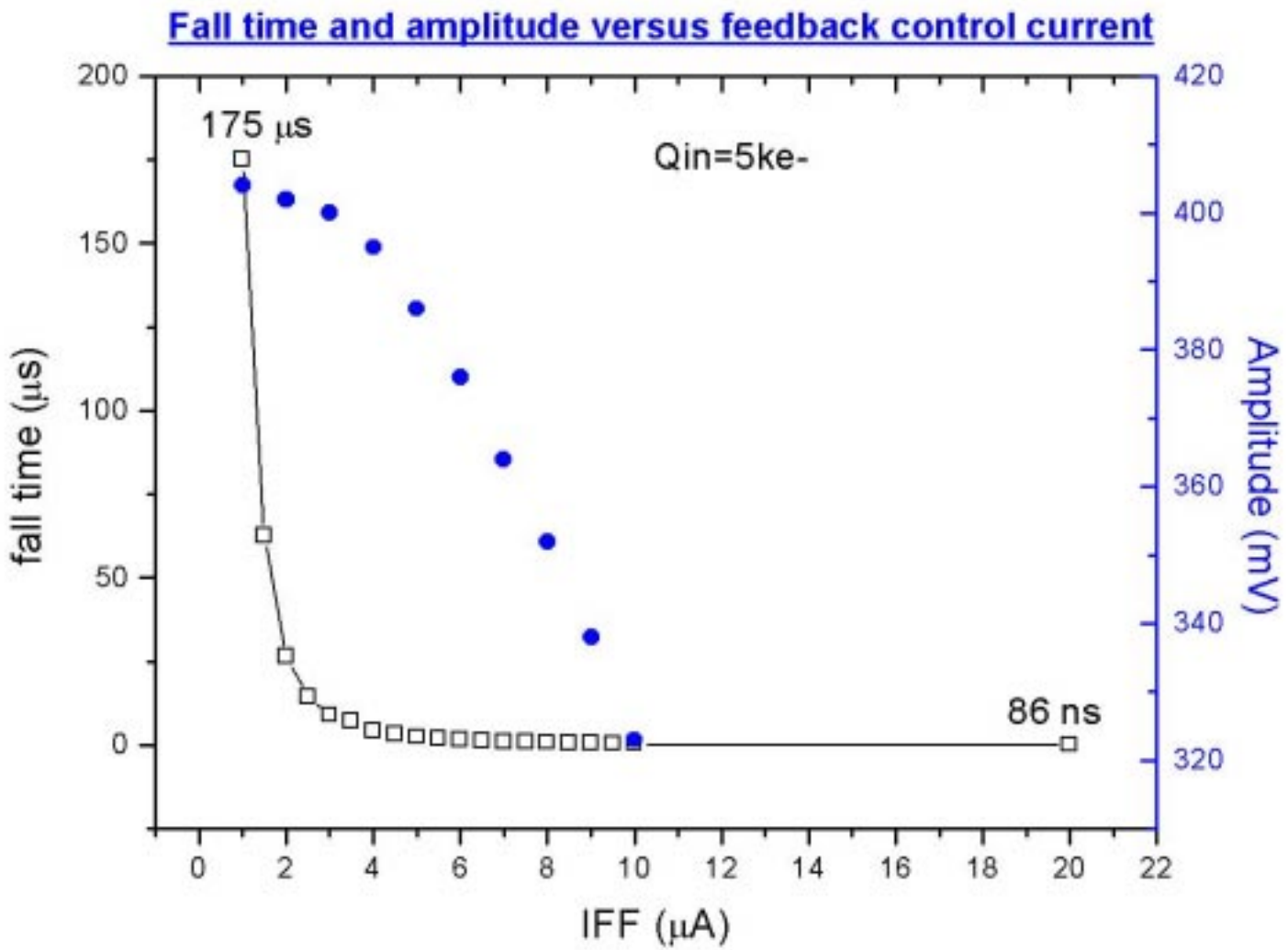
Typical front-end response

Buffered output of the second stage

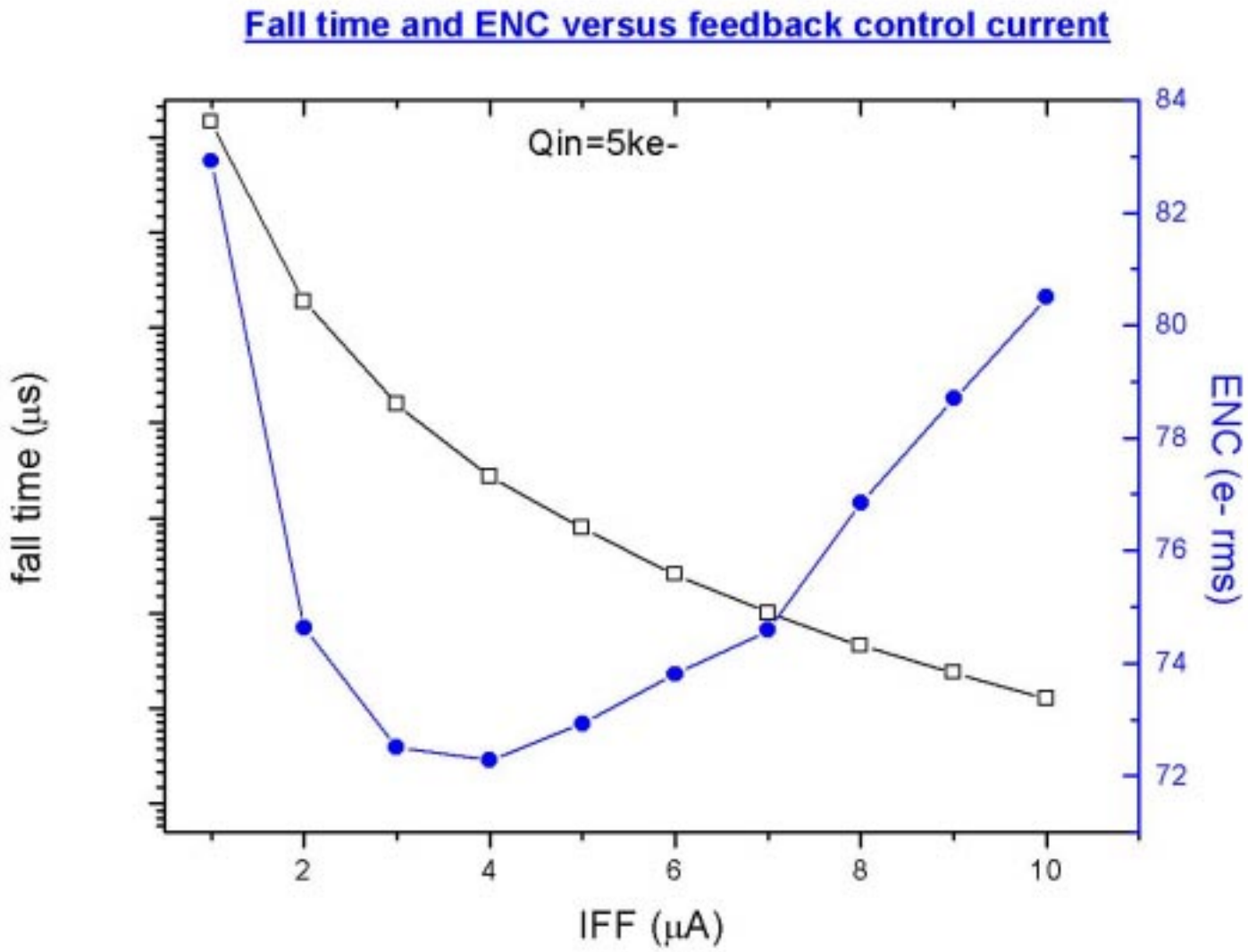
Feedback control



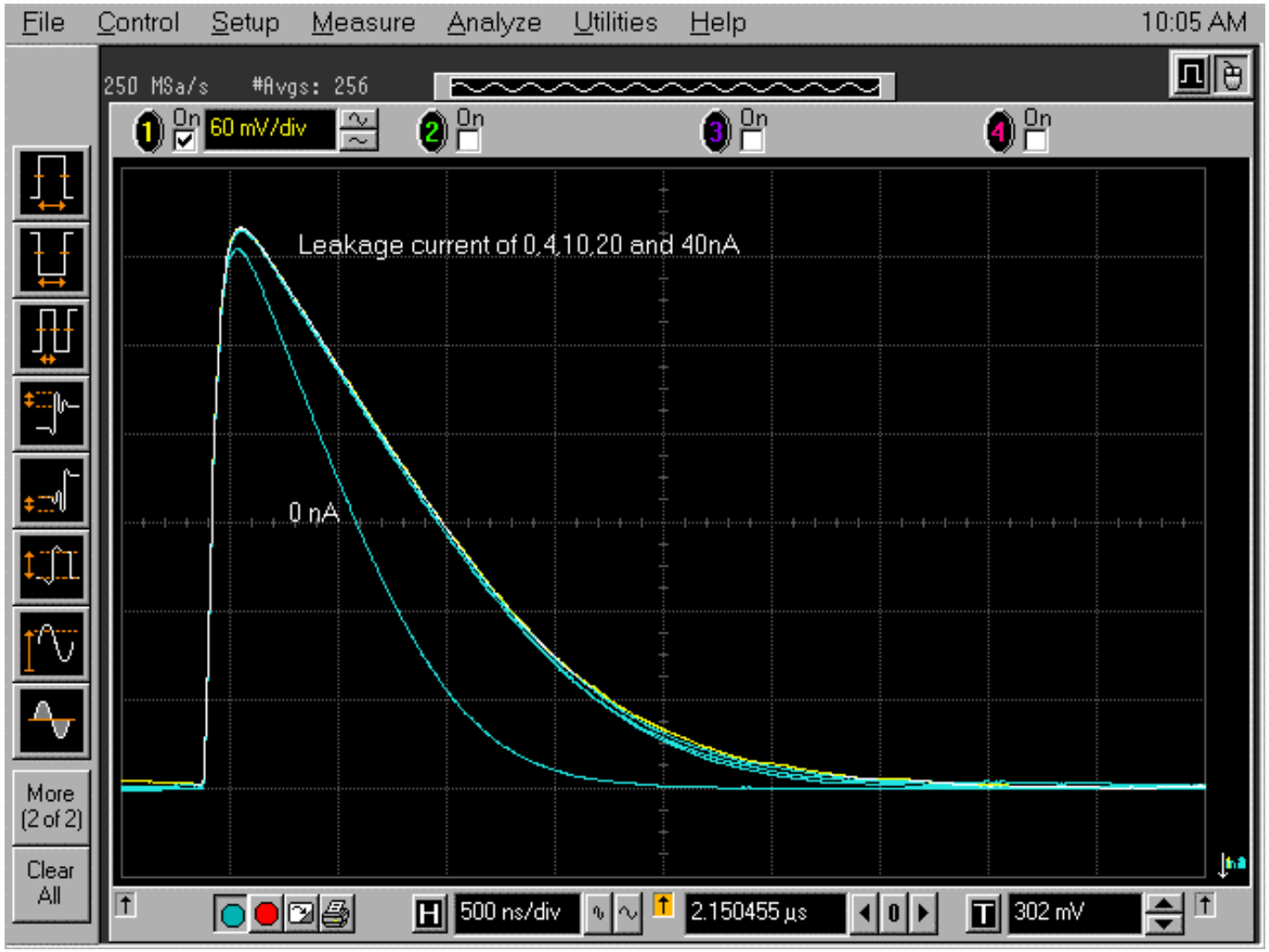
Feedback control



Feedback control

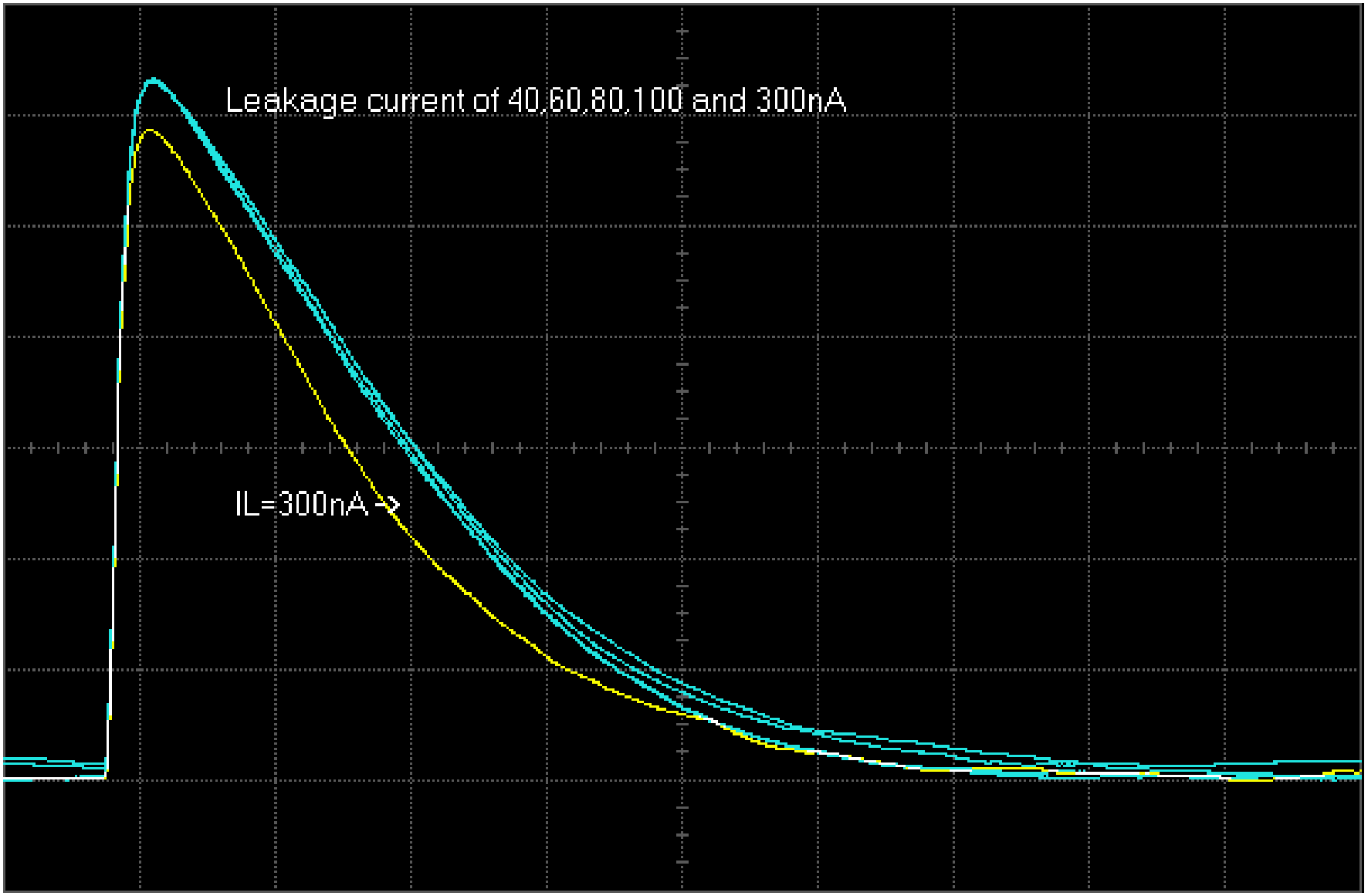


Leakage current compensation

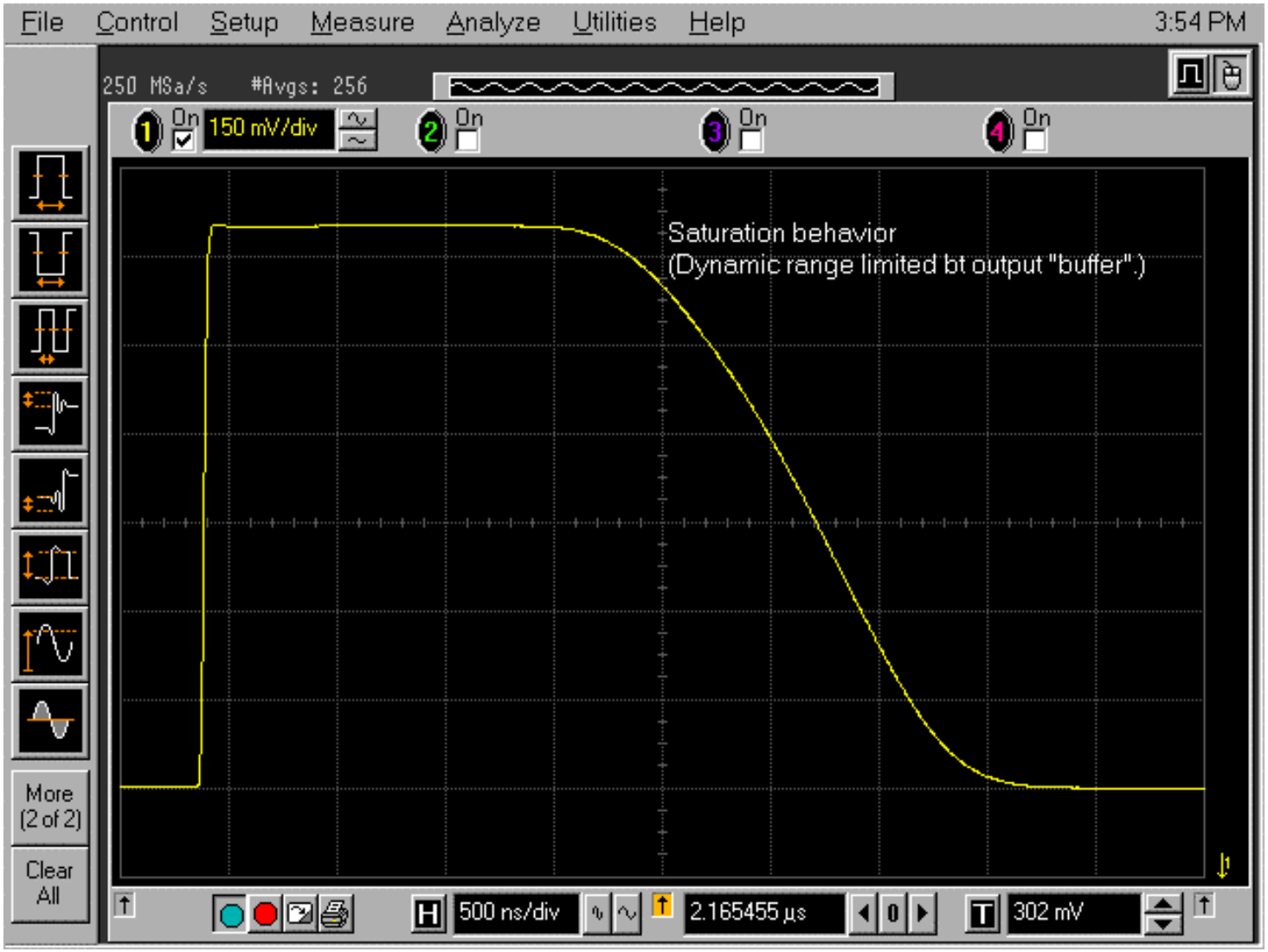


After the first nA no change in the response is observed !

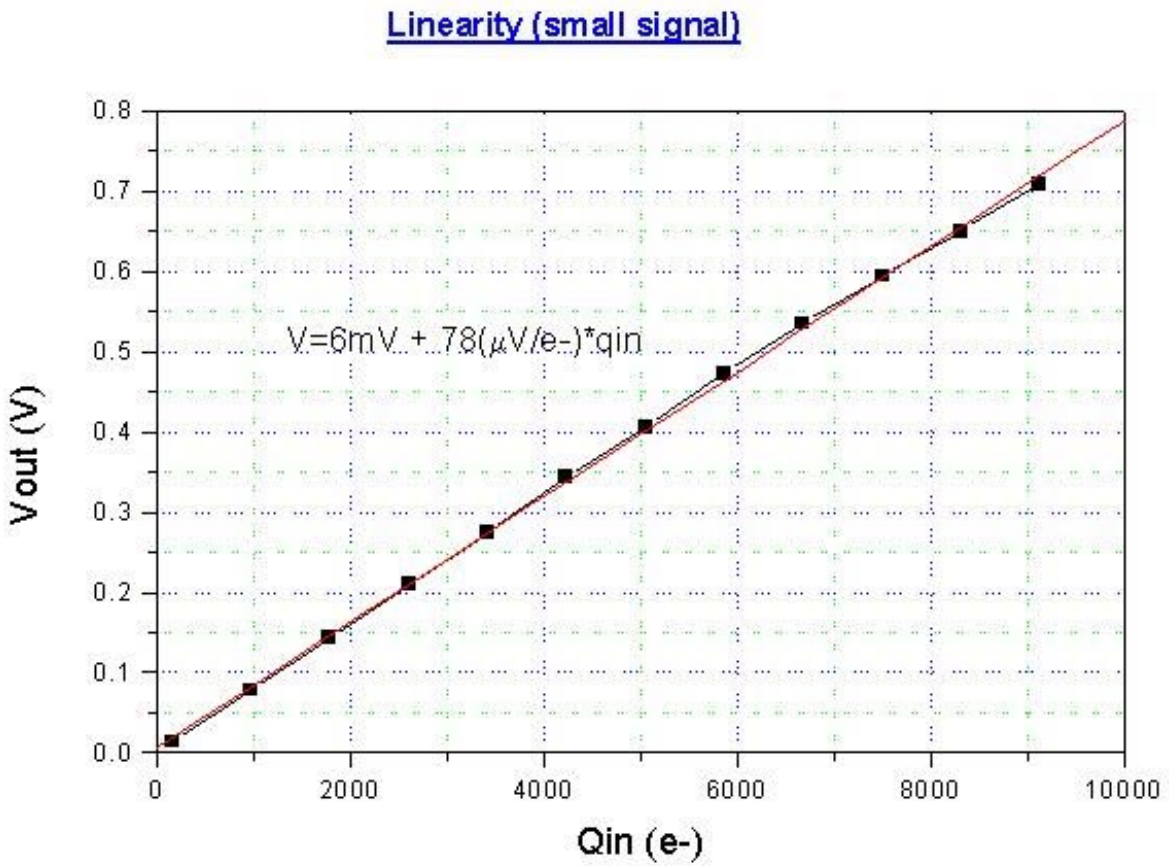
Leakage current compensation II



Response to large signals



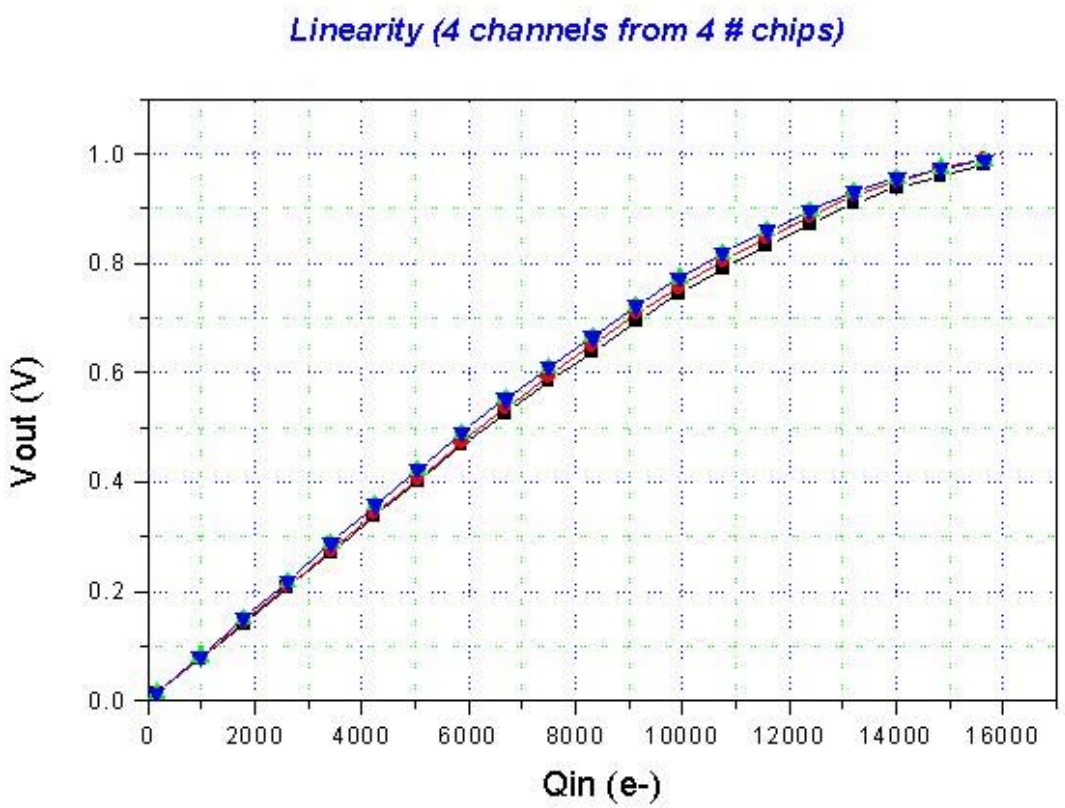
Linearity (small signals)



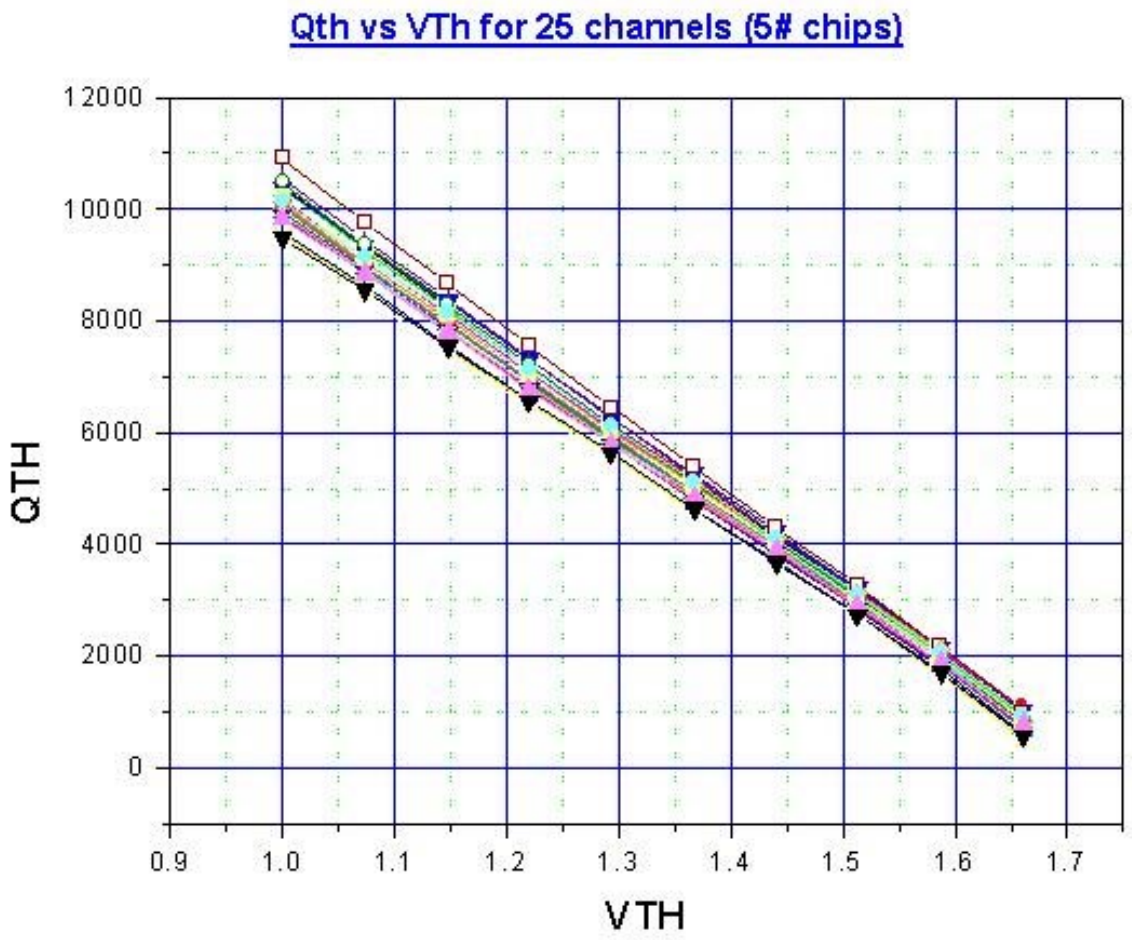
=> Ideal gain = (1/cf)(Cc2/cf2) = (1/8fF)*4 = 80 μV/e-

=> Spice predicted gain = 76 μV/e-

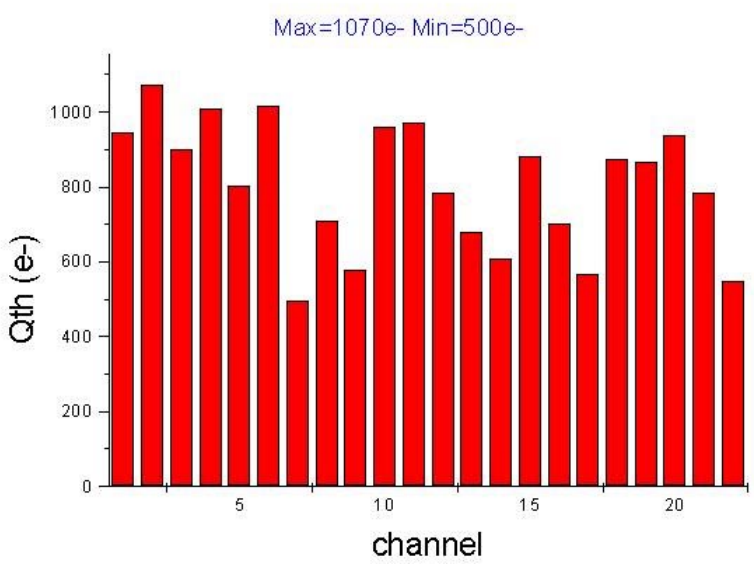
Linearity (larger signals)

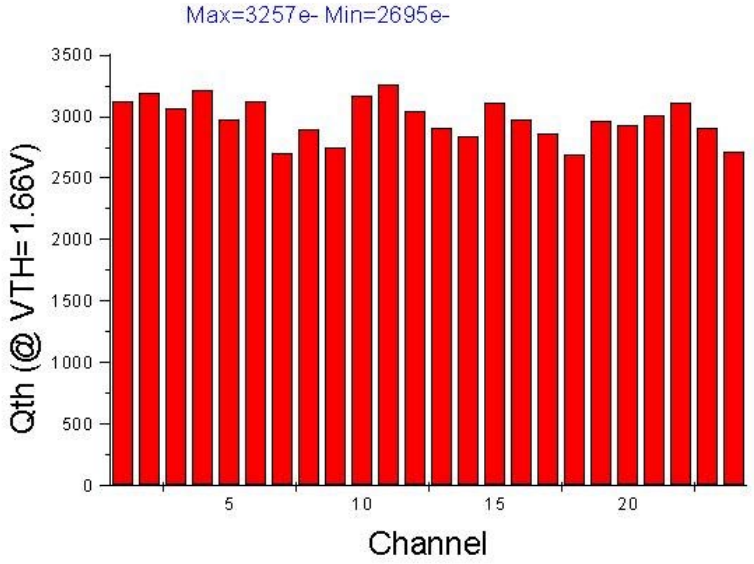


Threshold control and matching



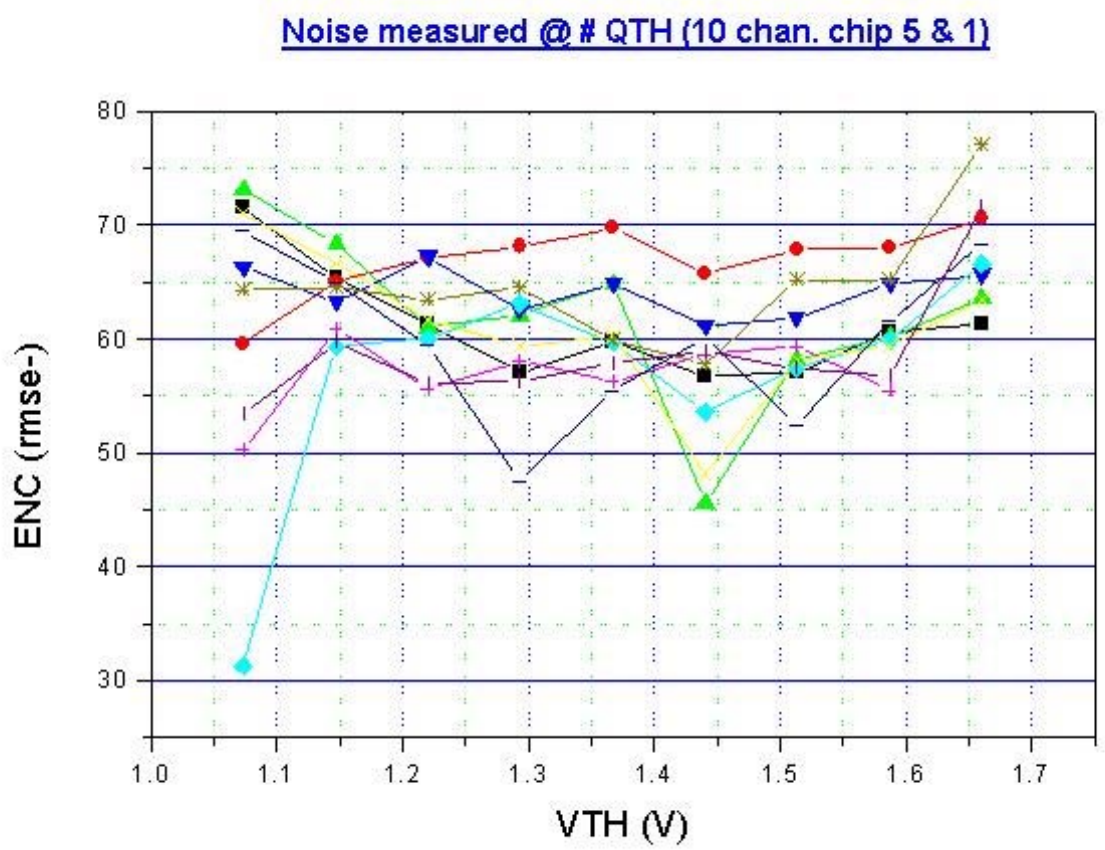
Threshold control and matching II





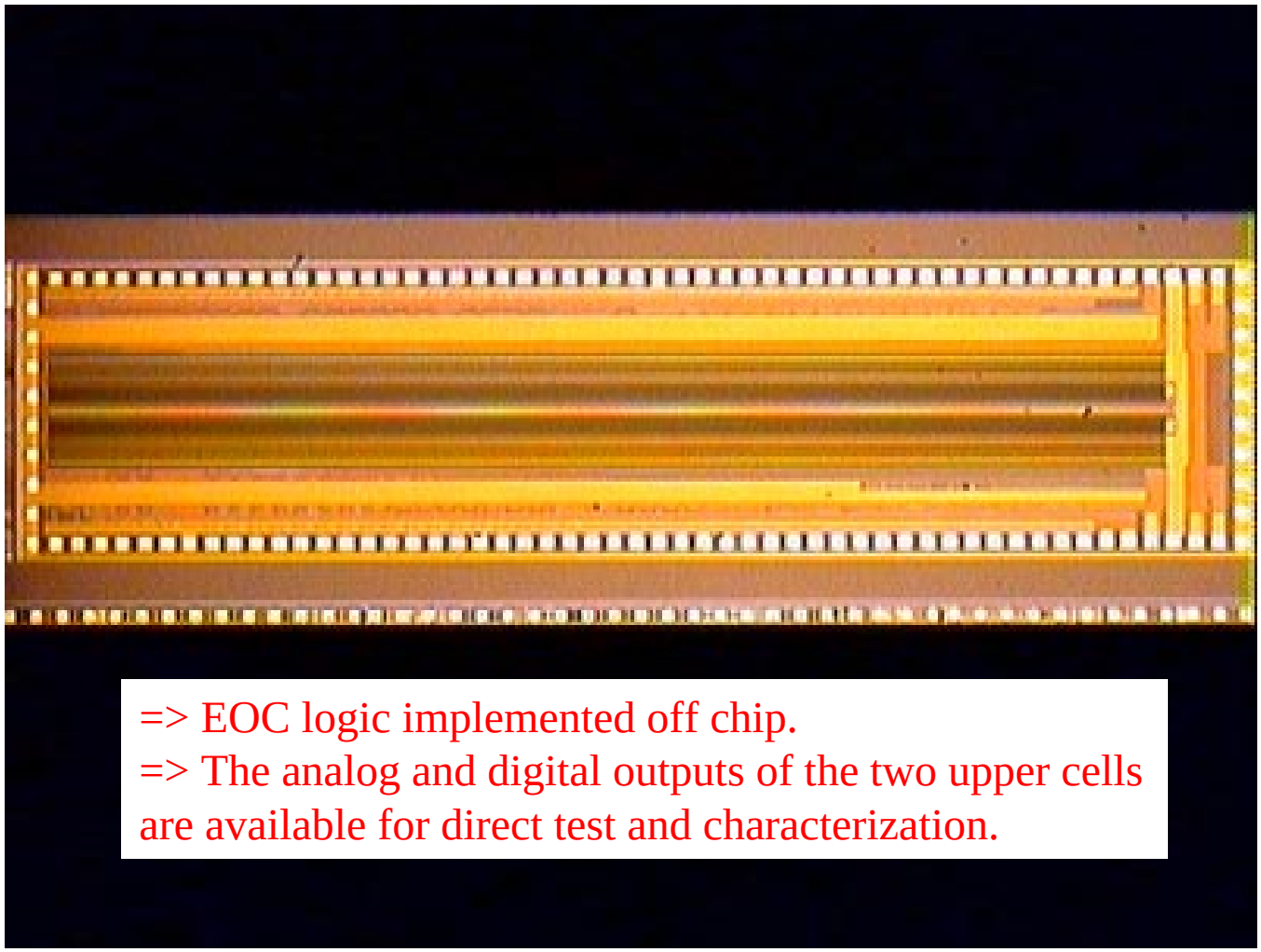
=> 25 channels from 5 different boards.

Noise (measured from efficiency curves)



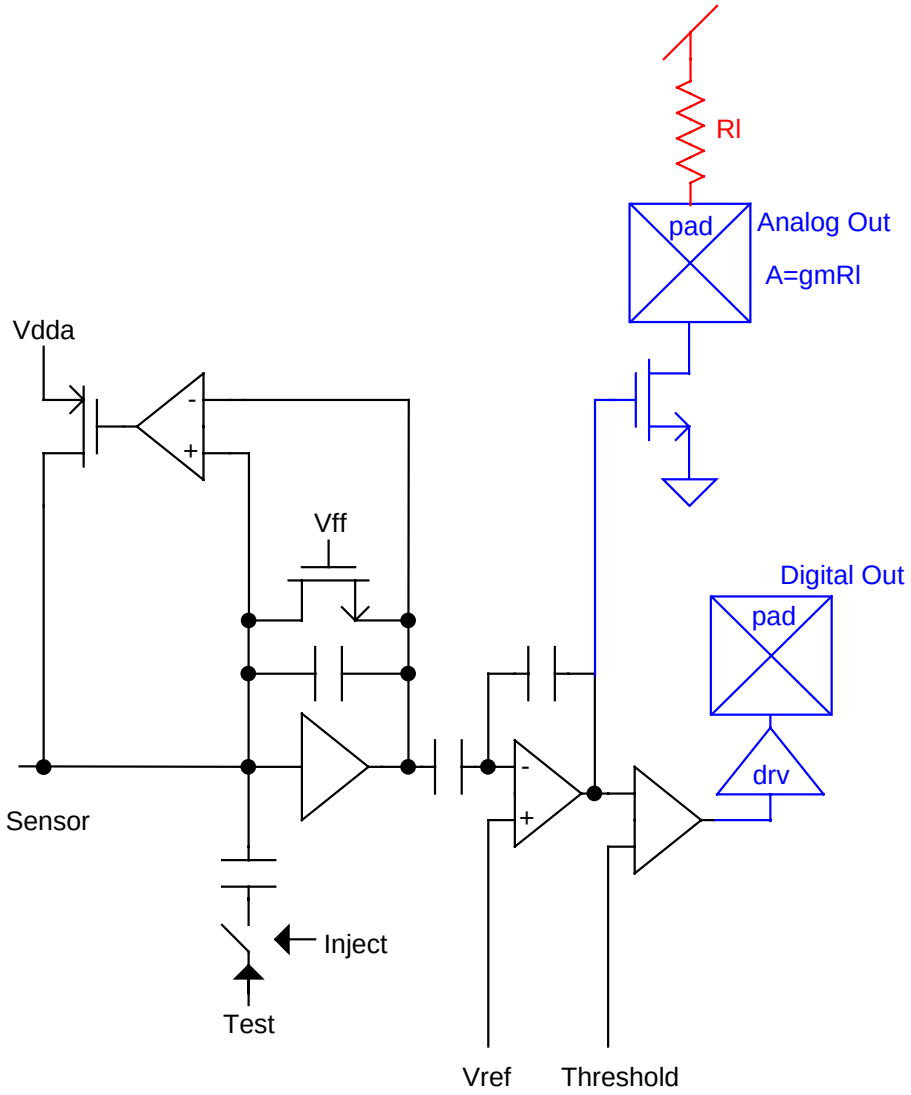
PreFPIX2_T

PreFPIX2_T is 2X160 pixel array. Each pixel cell contains all the functions needed for the BTEV experiment: kill and Inject logic, 3bit FADC, hit buffering, fast sparse RO.

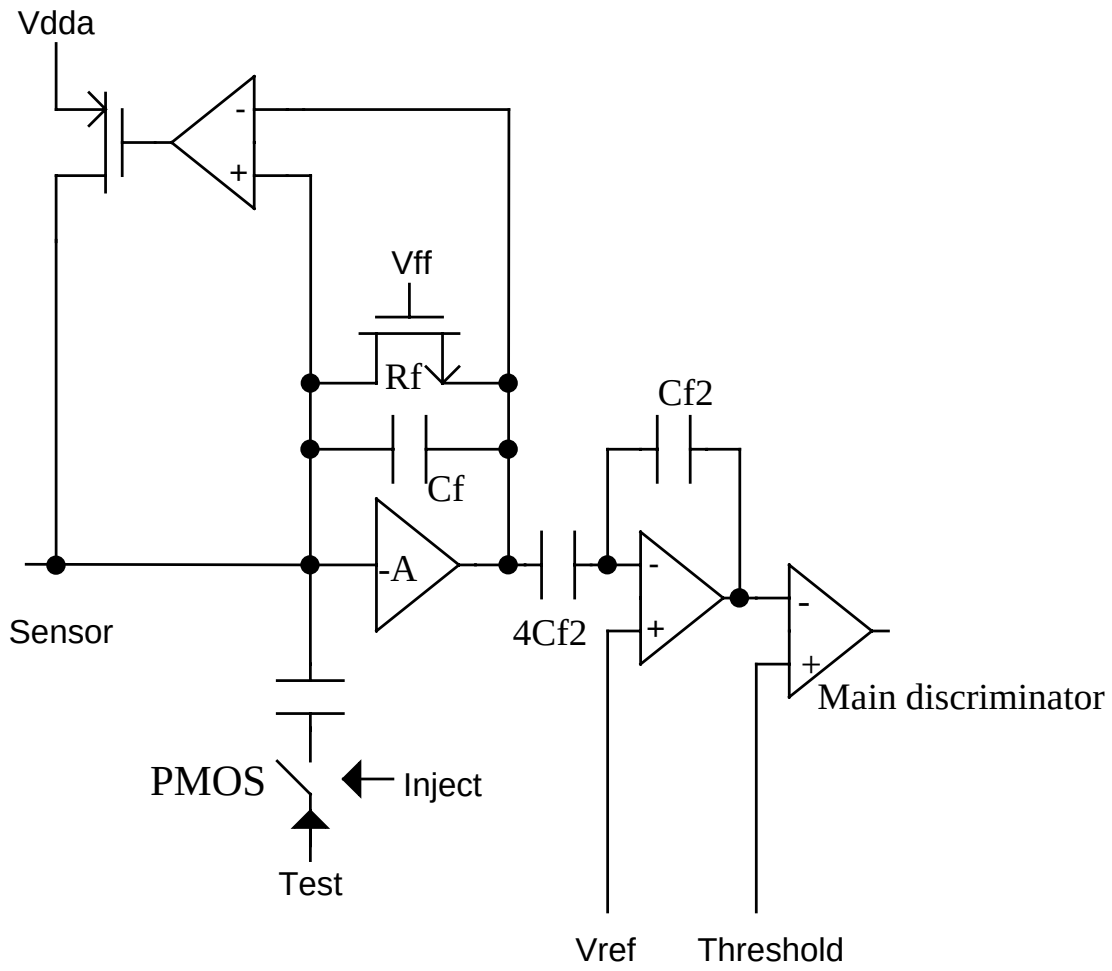


=> EOC logic implemented off chip.
=> The analog and digital outputs of the two upper cells are available for direct test and characterization.

Top cell buffered outputs

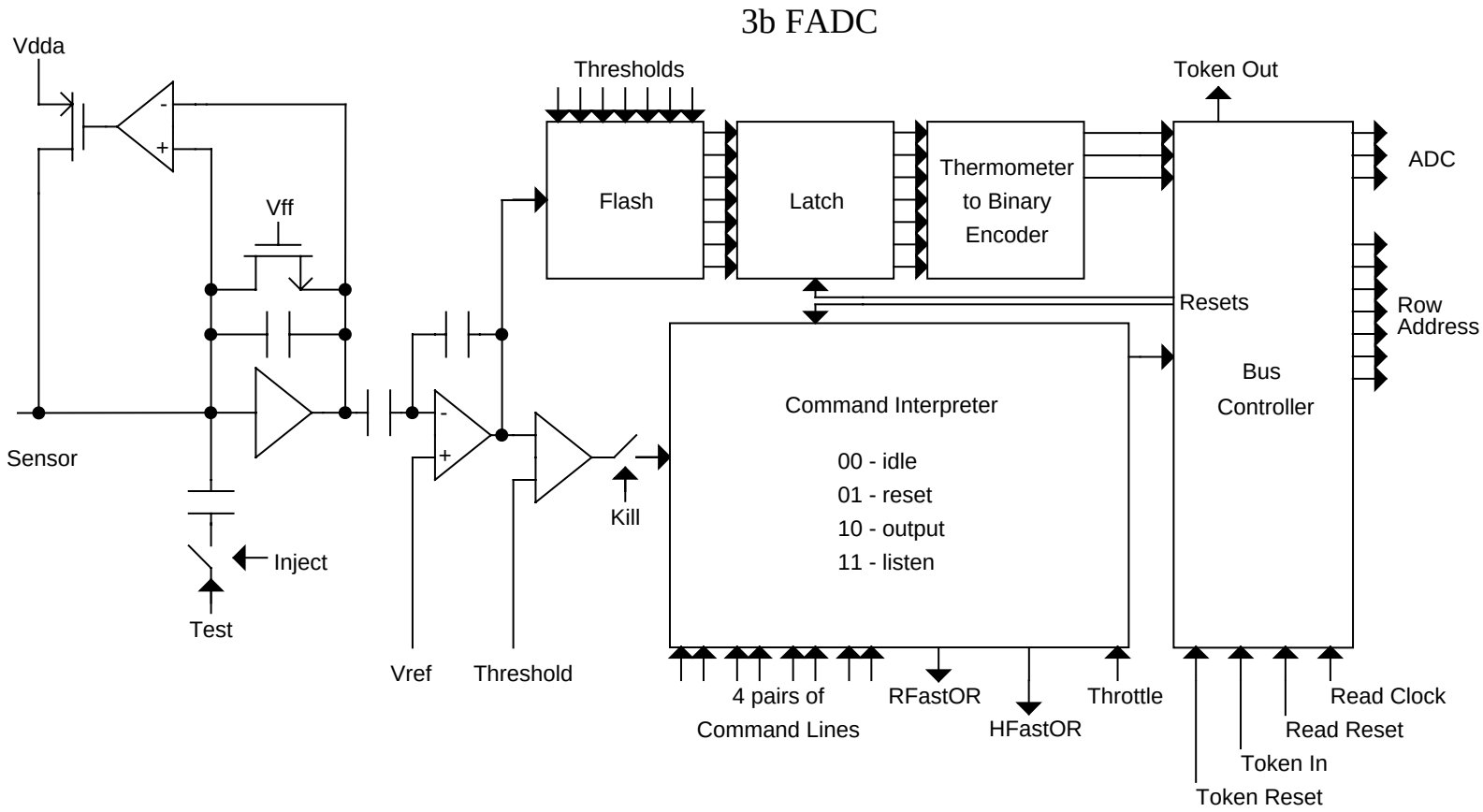


preFPIX2_T front-end



Same FE as preFPIX2 except that the injection transitor is a PMOS and the injection cap is realized with m1/m2 sandwich (2.6fF) instead of m1/poly (4fF). 2nd stage feedback “resistor” not shown.

preFPIX2_T pixel cell



PreFPIX2_T: pulse shapes

Irradiation of the PreFPIX2_T

- We have irradiated several test structures from two 0.25μ processes, from TSMC and a domestic vendor.
- Besides the individual devices we have irradiated also the prefPIX2 and preFPIX2_T pixel circuits
- The irradiation took place at the Co^{60} irradiation facility of the Argonne National Lab.
- A complete report on the results is still under preparation.
- Partial and VERY preliminary results from the test of the preFPIX2_T will be presented today.

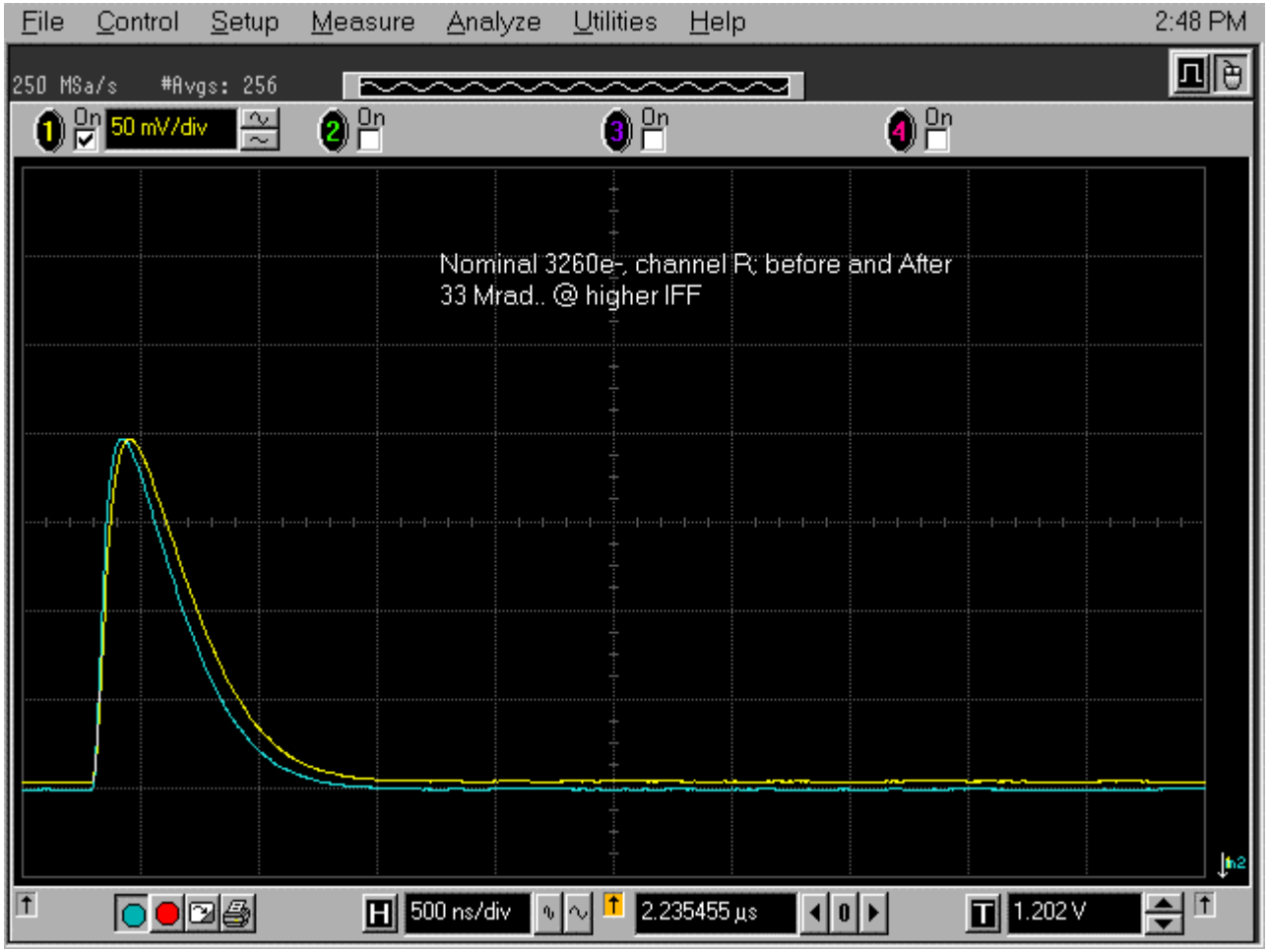
- Dosimetry accurate to 20%.
- No filter for low energy particles was used.
- All the results shown are after 1 to 7 days of annealing at room temperature.
- In all subsequent slides rad should read $rad(SiO_2)$

General effects after 33 Mrad

- Chip fully functional
- No degradation in speed (as inferred from the kill/inject shift register operation).
- Less than 10% change in “analog” power. Power was less after irradiation. Understandable from circuit point of view and is due to small VT change in the PMOS (<50 mV).

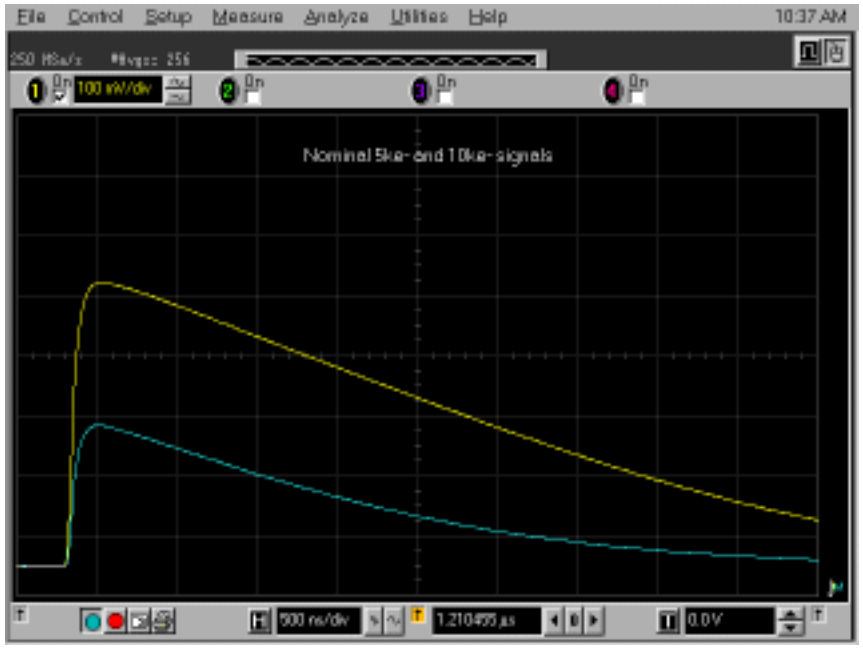
Total dose effects on front-end

Total dose effects on front-end

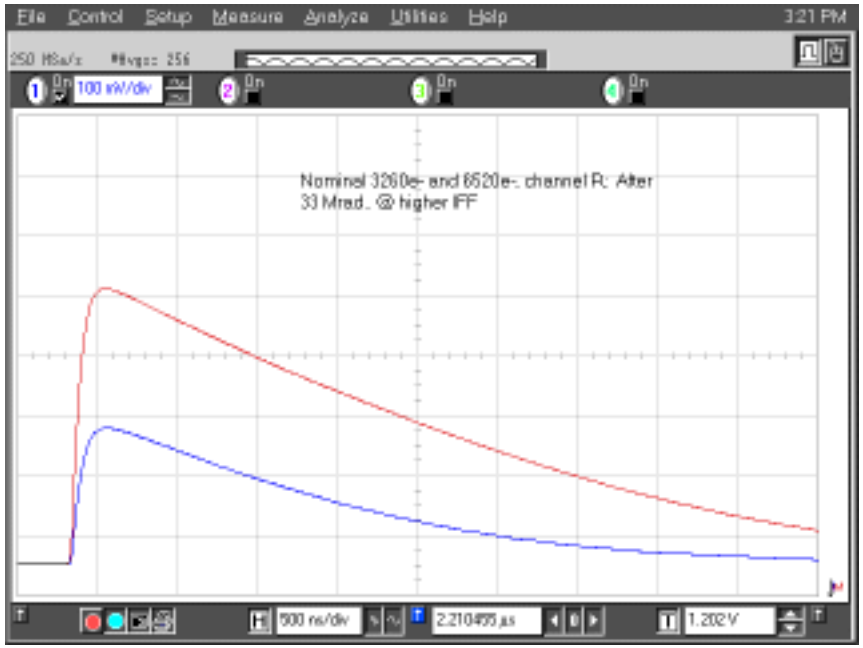


Total dose effects on front-end

Before irradiation

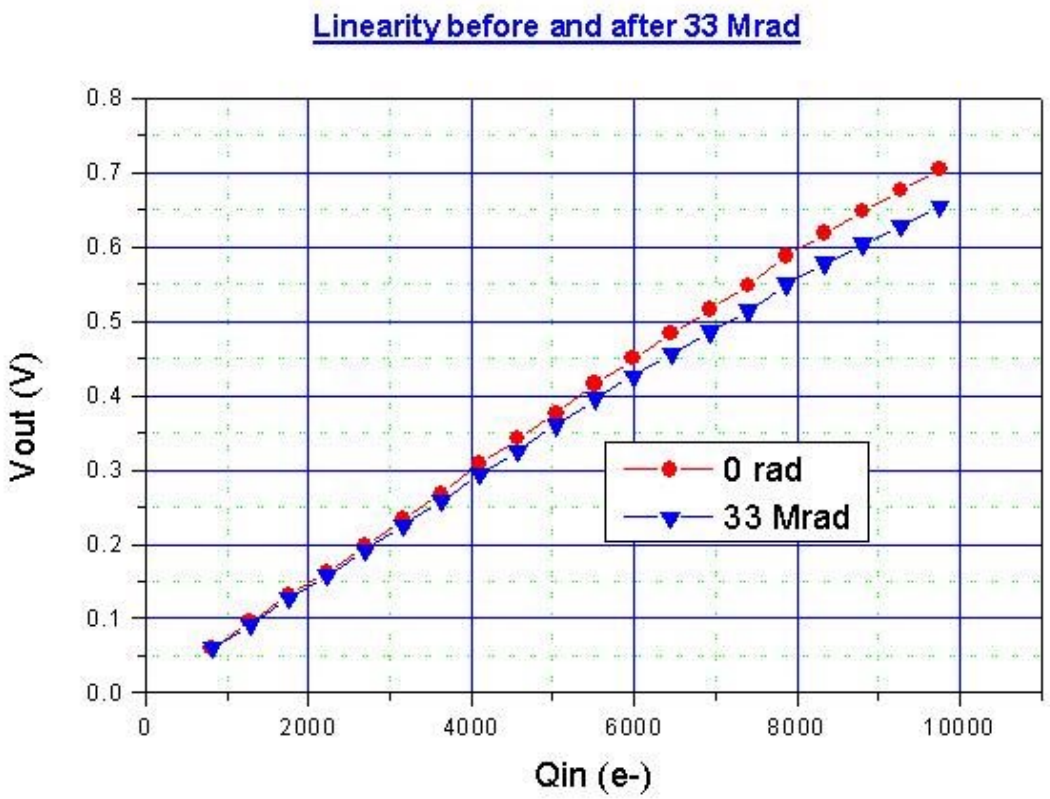


After 33 Mrad



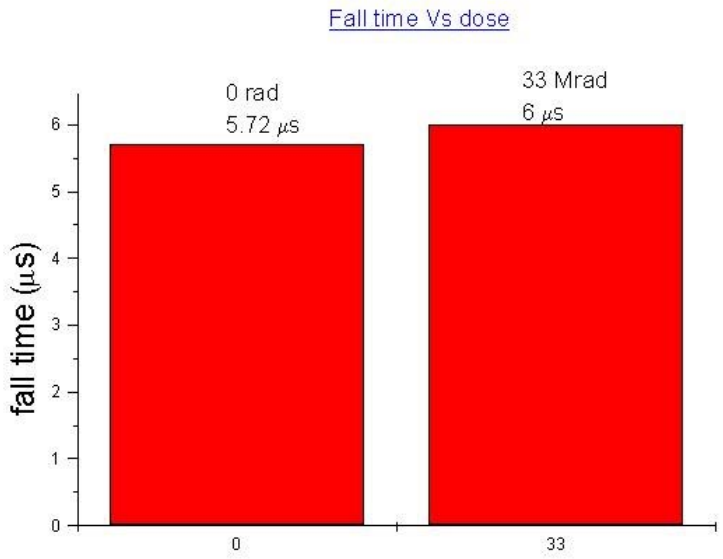
=> 3 mV DC offset shift (due mainly to output buffer)
=> < 4% Rise time difference
=> < 5% change in fall time.

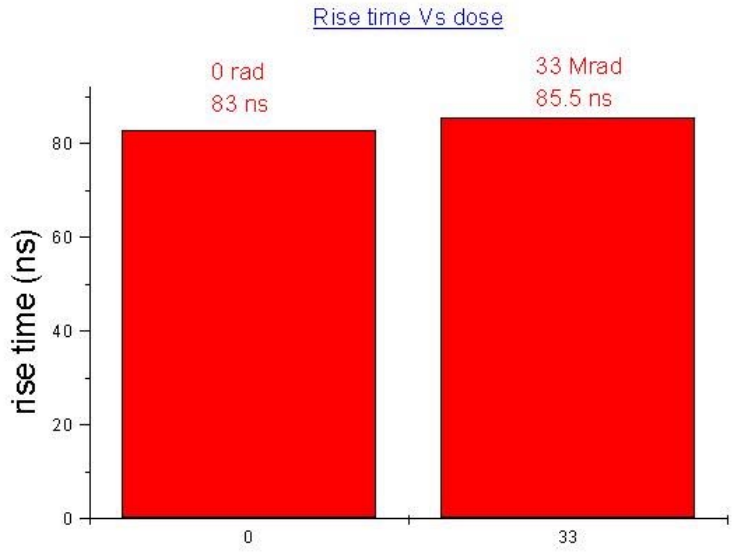
Linearity before and after 33 Mrad



=> 7 % max gain error. Believed to be due to output buffer only.

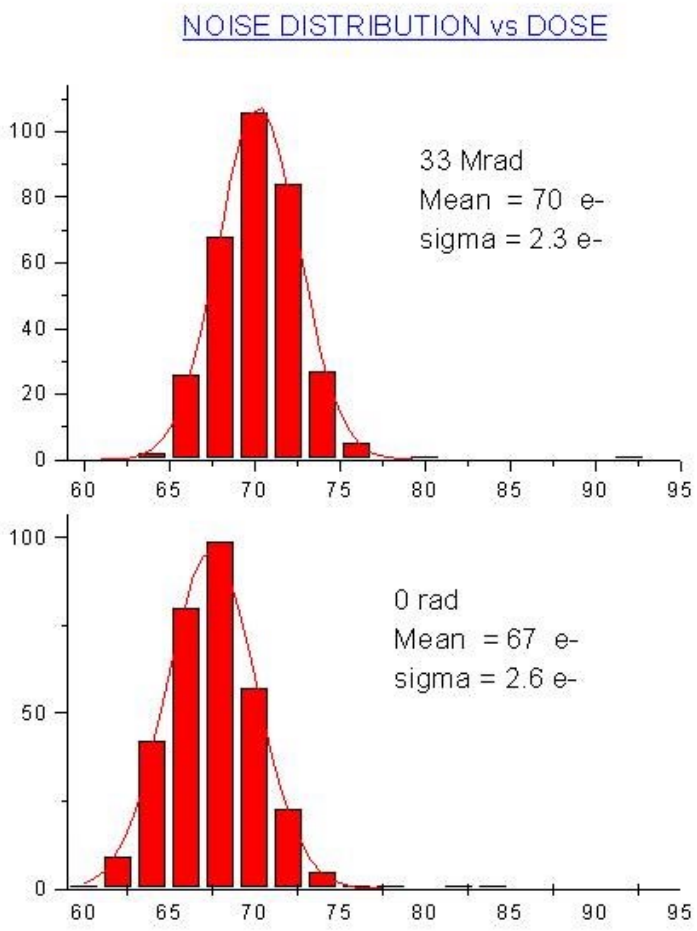
Rise and fall time before and after 33 Mrad

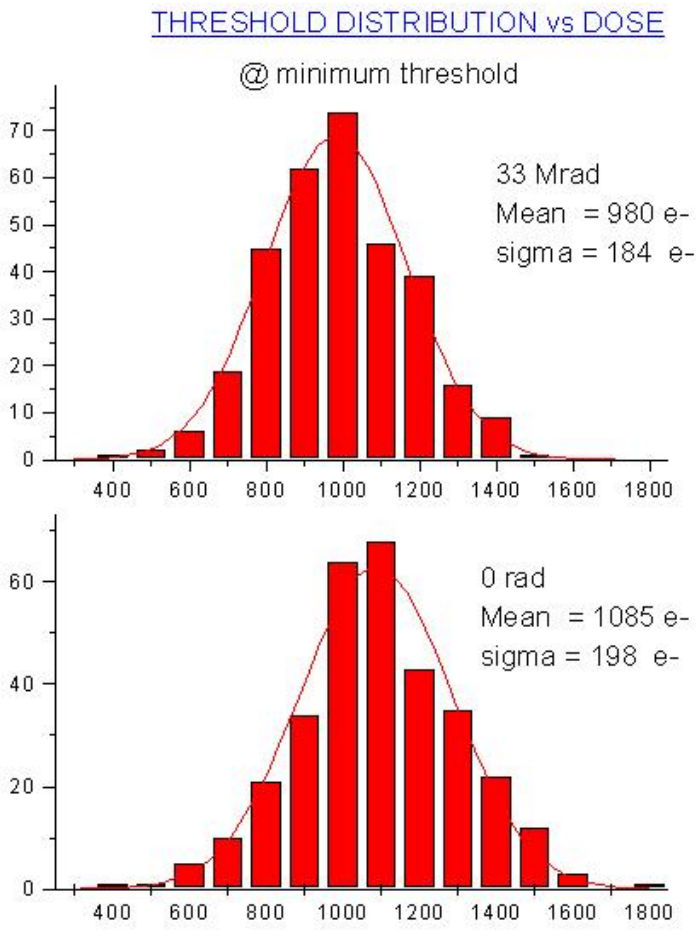




=> Changes are minimal and may disappear after annealing.

Noise and threshold distributions

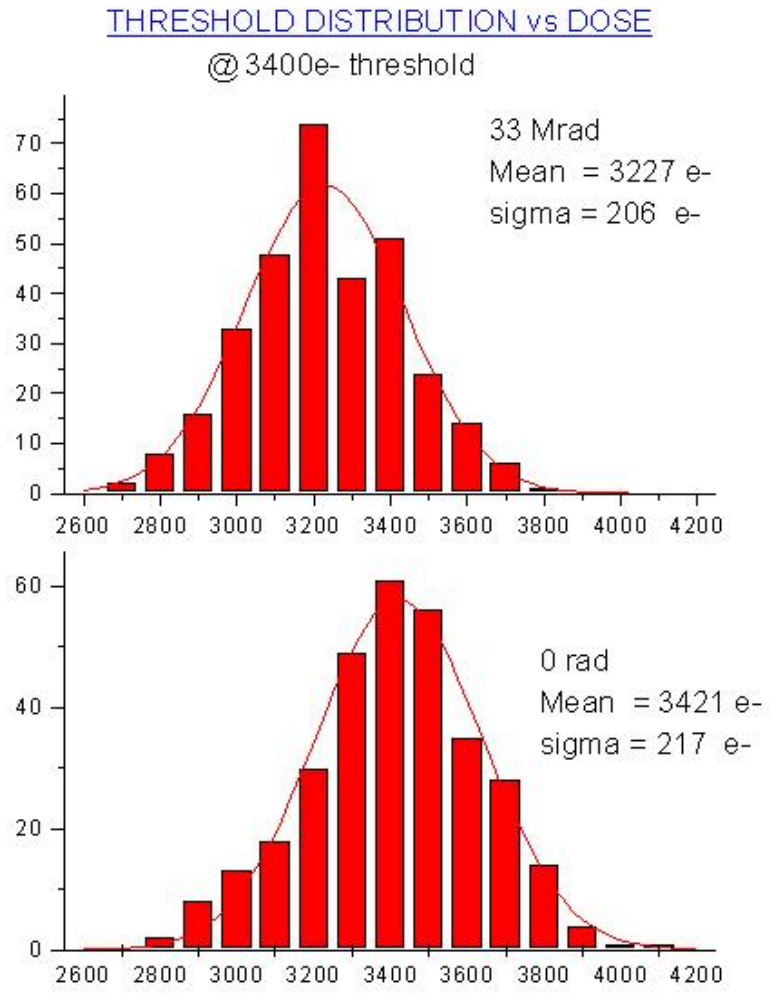




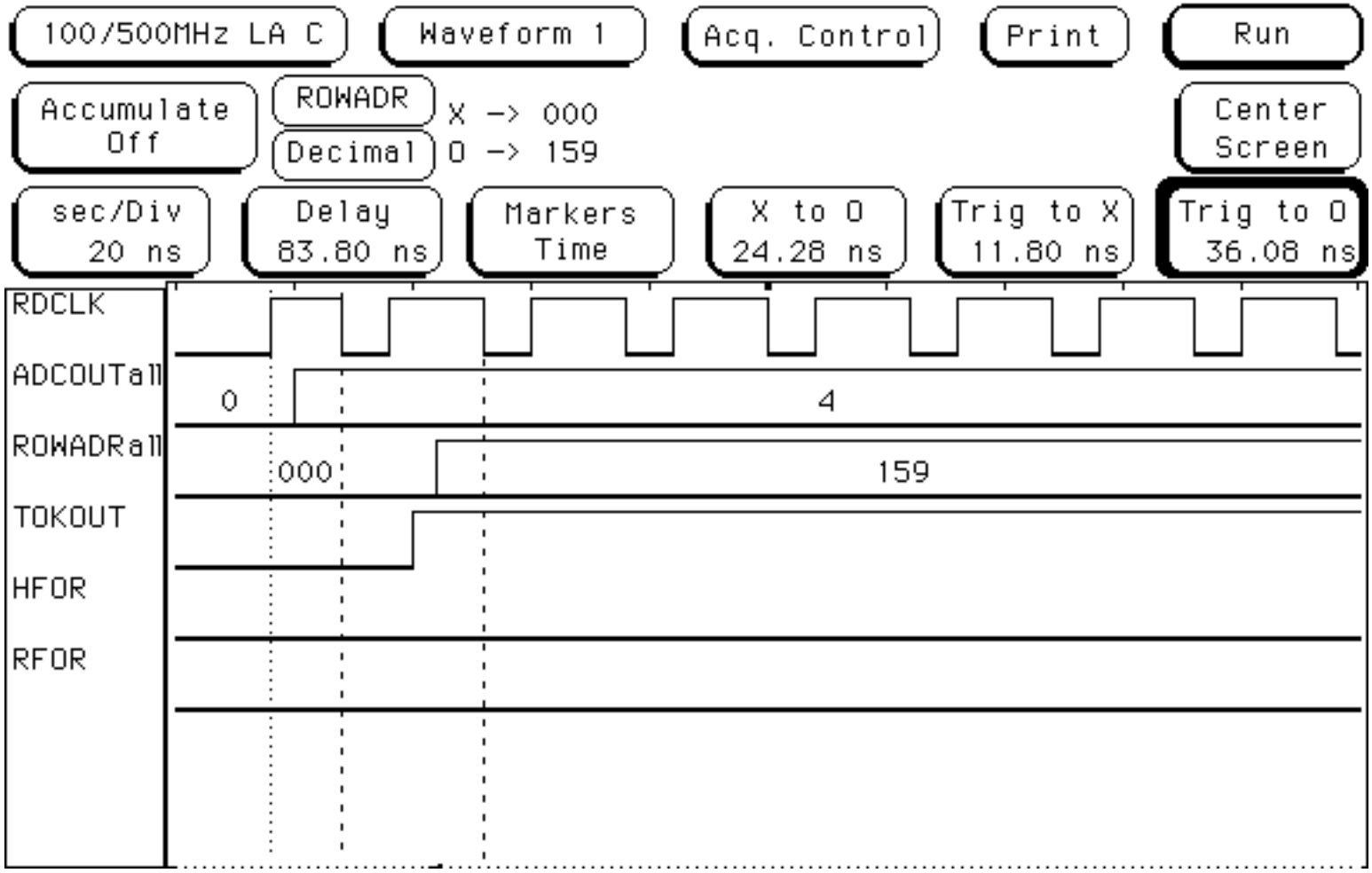
=> Practically no change in noise and threshold dispersion.

=> 200 e- change in the threshold voltage.

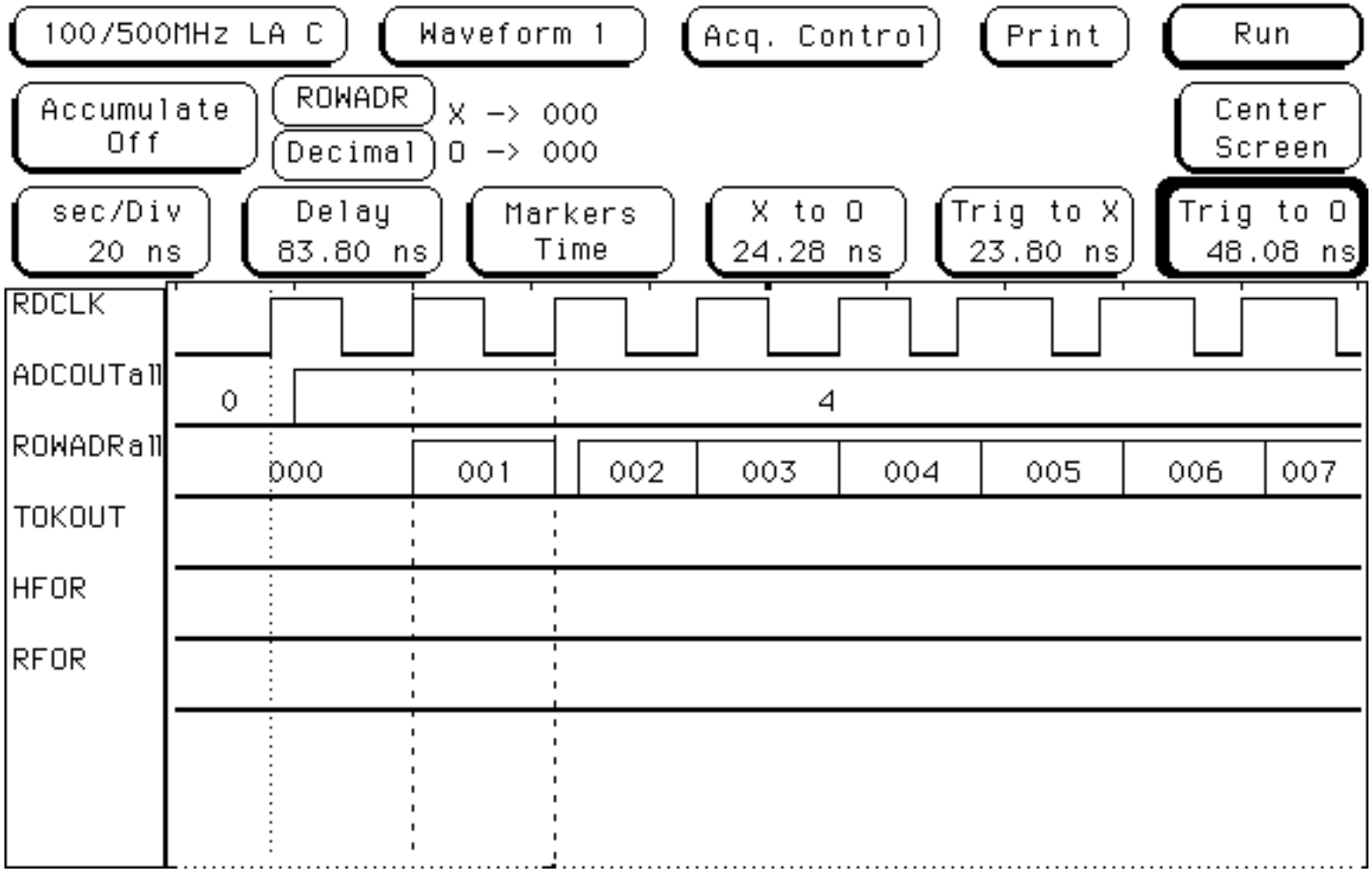
Effects at higher threshold



Readout typical output



Readout Max speed



Conclusions

- We successfully migrated our design from 0.5µ process to 0.25µ using radiation tolerant techniques.
- The design can be submitted to two different vendors.
- Chip performed as expected before and after 33 Mrad.
- We are still working on the radiation results.
- DSM is the way to go for radiation hardness (if you can).

Acknowledgements

- William Wester co-organizer of the irradiation “week”.
- Tory Steed and Al. Al Svirmickas from ANL for their precious help.
- Al Deyer and Kelly Knickerbocker for preparing the boards and the 100’s of feet of cable.
- Ray Yarema for his advice and encouragements.